Please replace the Abstract with the following:

ABSTRACT

A method and system for performing switch operations utilize non-architectural registers to store context information. Data in a first context register on a peripheral system is ~~access~~ <u>accessed</u> (e.g., read or write) until a host computer provides a new index value to an index register on the peripheral system. A context switch occurs, and the context register associated with the new index value is accessed. [[]] <u>In some embodiments a</u> [[A]] system that performs context switching includes a host computer, at least one peripheral system coupled to the host computer, an interface between the host computer and the peripheral system, and a register access circuit coupled to the host computer. The register access circuit is configured to access data in a first <u>or a second</u> register on the peripheral system if the first <u>or a second</u> index value<u>, respectively,</u> is provided by the host computer<u>.</u> ~~and is further configured to access data in a second register of a peripheral system if the second index value is provided by the host computer. In at least one embodiment of the system, the first and second registers are not architected registers.~~

A replacement sheet is enclosed.

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ABSTRACT

A method and system for performing switch operations utilize non-architectural registers to store context information. Data in a first context register on a peripheral system is accessed (e.g., read or write) until a host computer provides a new index value to an index register on the peripheral system. A context switch occurs, and the context register associated with the new index value is accessed. In some embodiments a system that performs context switching includes a host computer, at least one peripheral system coupled to the host computer, an interface between the host computer and the peripheral system, and a register access circuit coupled to the host computer. The register access circuit is configured to access data in a first or a second register on the peripheral system if the first or a second index value, respectively, is provided by the host computer.

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